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SELF- ALIGNED ARRAY CONTACT FOR MEMORY CELLS

Abstract

A method of forming bitlines for a memory cell array of an integrated circuit and conductive lines interconnecting transistors of an external region outside of the memory cell array is provided. The method includes patterning troughs in a dielectric region covering the memory cell array according to a first critical dimension mask. Bitline contacts to a substrate and bitlines are formed in the troughs. Thereafter, conductive lines are formed which consist essentially of at least one material selected from the group consisting of metals and conductive compounds of metals in horizontally oriented patterns patterned by a second critical dimension mask, wherein the conductive lines interconnect the bitlines to transistors of external circuitry outside of the memory cell array, the conductive lines being interconnected to the bitlines only at peripheral edges of the memory cell array.